Alessandro TEMPIA CALVINO

Ph.D. Candidate

1020 Renens - Switzerland
(+41) 762 13 40 59
alessandro.tempiacalvino@epfl.ch
https://aletempiac.github.io
alessandro-tempia-calvino
Google scholar

I am a Doctoral Candidate in the department of Computer and Communication Sciences at the Swiss Federal Institute of Technology of Lausanne (EPFL). My research interests include electronic design automation, logic synthesis, and emerging technologies.

Education

Sep 2020 – pres: **Doctor of Philosophy - Ph.D. in Computer and Communication Sciences**, *EPFL (École Polytechnique Fédérale de Lausanne)*, Lausanne, Switzerland.
Thesis advisor: Prof. Giovanni De Micheli

Sep 2018 – Sep 2020: **Master of Science in Computer Engineering**, *Télécom Paris*, EURECOM - Biot, France.
Specialization in Smart Objects - joint master program with Politecnico di Torino, **GPA 4.0/4**

Sep 2017 – Mar 2020: **Master of Science in Computer Engineering**, *Politecnico di Torino*, Torino, Italy.
Specialization in Embedded Systems - joint master program with Télécom Paris, **Full marks with honor (110 cum laude/110)**

Sep 2014 – Sep 2017: **Bachelor's Degree in Computer Engineering**, *Politecnico di Torino*, Torino, Italy.

Experience

Sep 2020 – pres: **Doctoral Researcher**, *EPFL (École Polytechnique Fédérale de Lausanne)*, Lausanne, Switzerland.
Integrated Systems Laboratory - Electronics design automation (EDA), logic synthesis, and emerging technologies.

Jun 2022 – Oct 2022: **Research Intern**, *X, the Moonshot Factory (Google X)*, Mountain View, USA.
Logic synthesis and EDA.

Mar 2020 – Aug 2020: **R&D Engineer**, *Télécom Paris*, EURECOM - Biot, France.
Implementation of a model-checker for embedded system models.

Jul 2019 – Dec 2019: **Intern**, *Synopsys*, Montbonnot-Saint-Martin, France.
Implementation of timing-driven algorithms for the synthesis of digital circuits.

Publications

Conference and Workshop Papers:

- S.-Y. Lee, **A. Tempia Calvino**, H. Riener, G. De Micheli, "Late Breaking Results: Majority-Inverter Graph Minimization by Design Space Exploration", accepted in Design Automation Conference (DAC), 2024.
- **A. Tempia Calvino**, G. De Micheli, A. Mishchenko, R. Brayton, "Practical Boolean Decomposition for Delay-driven LUT Mapping", accepted in International Workshop on Logic & Synthesis (IWLS), 2024.
- A. Costamagna, **A. Tempia Calvino**, A. Mishchenko, G. De Micheli, "Post-Mapping Resubstitution For Area-Oriented Optimization", accepted in International Workshop on Logic & Synthesis (IWLS), 2024.
- A. Costamagna, **A. Tempia Calvino**, A. Mishchenko, G. De Micheli, "Area-Oriented Resubstitution For Networks of Look-Up Tables", accepted in International Workshop on Logic & Synthesis (IWLS), 2024.
- **A. Tempia Calvino**, G. De Micheli, "Scalable Logic Rewriting Using Don't Cares", in Design Automation and Test in Europe Conference (DATE), 2024.
- R. Bairamkulov, S.-Y. Lee, **A. Tempia Calvino**, D. Marakkalage, M. Yu, G. De Micheli, "Technology-Aware Logic Synthesis for Superconductive Electronics", in Design Automation and Test in Europe Con-

ference (DATE), 2024.
- **A. Tempia Calvino**, G. De Micheli, "Algebraic and Boolean Methods for SFQ Superconducting Circuits", in Asian and South Pacific Design Automation Conference (ASP-DAC), 2024.
- G. Radi, **A. Tempia Calvino**, G. De Micheli, "In Medio Stat Virtus: Combining Boolean and Pattern Matching", in Asian and South Pacific Design Automation Conference (ASP-DAC), 2024.
- **A. Tempia Calvino**, G. De Micheli, "Technology Mapping Using Multi-output Library Cells", in IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2023.
- R. Bairamkulov, **A. Tempia Calvino**, G. De Micheli, "Synthesis of SFQ Circuits with Compound Gates", in 2023 IFIP/IEEE 31st International Conference on Very Large Scale Integration (VLSI-SoC), 2023.
- **A. Tempia Calvino**, A. Mishchenko, H. Schmit, E. Mahintorabi, G. De Micheli, X. Xu, "Improving Standard-Cell Design Flow using Factored Form Optimization", in ACM/IEEE Design Automation Conference (DAC), 2023.
- **A. Tempia Calvino**, G. De Micheli, "Technology Mapping Using Multi-output Library Cells", in International Workshop on Logic & Synthesis (IWLS), 2023.
- A. Mishchenko, R. Brayton, **A. Tempia Calvino**, G. De Micheli, "Boolean Decomposition Revisited", in International Workshop on Logic & Synthesis (IWLS), 2023.
- **A. Tempia Calvino**, G. De Micheli, "Depth-Optimal Buffer and Splitter Insertion and Optimization in AQFP Circuits", in Asian and South Pacific Design Automation Conference (ASP-DAC), 2023.
- **A. Tempia Calvino**, G. De Micheli, "Depth-optimal Buffer and Splitter Insertion and Optimization in AQFP Circuits", in International Workshop on Logic & Synthesis (IWLS), 2022.
- G. Meuli, V. Possani, R. Singh, S.-Y. Lee, **A. Tempia Calvino**, D. Marakkalage, P. Vuillod, L. Amarù, S. Chase, J. Kawa, and G. De Micheli, "Majority-based design flow for AQFP superconducting family", in Design Automation and Test in Europe Conference (DATE), 2022.
- L. Apvrille, P. de Saqui-Sannes, O. Hotescu, **A. Tempia Calvino**, "SysML models verification relying on dependency graphs", in International Conference on Model-Driven Engineering and Software Development (MODELSWARD), 2022.
- **A. Tempia Calvino**, H. Riener, S. Rai, G. De Micheli, "A versatile mapping approach for technology mapping and graph optimization", in Asian and South Pacific Design Automation Conference (ASP-DAC), 2022.
- **A. Tempia Calvino**, H. Riener, S. Rai, G. De Micheli, "From logic to gates: A versatile mapping approach to restructure logic", in International Workshop on Logic & Synthesis (IWLS), 2021.
- **A. Tempia Calvino**, L. Apvrille, "Direct model-checking of SysML models", in International Conference on Model-Driven Engineering and Software Development (MODELSWARD), 2021.

Journal Papers and Book Chapters:
- **A. Tempia Calvino**, G. De Micheli, A Mishchenko, R. Brayton, "Enhancing Delay-driven LUT Mapping with Boolean Decomposition", in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), *under review*, 2024.
- S.-Y. Lee, **A. Tempia Calvino**, G. De Micheli, "Technology Legalization and Optimization for Adiabatic Quantum-Flux Parametron", in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), *under review*, 2024.
- R. Bairamkulov, **A. Tempia Calvino**, G. De Micheli, "Synthesis of SFQ Circuits with Compound Gates", in VLSI-SoC 2023, Springer, *accepted*, 2023.
- L. Apvrille, P. Saqui-Sannes, O.A. Hotescu, **A. Tempia Calvino**, "Dependency Graphs to Boost the Verification of SysML Models", in Model-Driven Engineering and Software Development, MODELSWARD 2021-2022, Springer, 2023.
- S. Rai, **A. Tempia Calvino**, H. Riener, G. De Micheli, A. Kumar, "Utilizing XMG-based Synthesis to Preserve Self-duality for RFET-based Circuits", in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2022.

Preprints:
- M. Soeken, H. Riener, W. Haaswijk, E. Testa, B. Schmitt, G. Meuli, F. Mozafari, S.-Y. Lee, **A. Tempia Calvino,** D. S. Marakkalage, G. De Micheli, "The EPFL logic synthesis libraries", arXiv preprint

arXiv:1805.05121v3, 2022.

Patents

- **A. Tempia Calvino**, Xiaoqing Xu, Herman Schmit, "Transistor-level synthesis", 2024.
- Xiaoqing Xu, Herman Schmit, **A. Tempia Calvino**, "Auto-creation of custom standard cells", 2024.

Invited and Conference Talks

Invited Talks:

- **A. Tempia Calvino**, "Technology-aware logic synthesis for superconducting electronics", in International Workshop on Quantum, Cryogenic and Superconductive Computing, *scheduled*, 2024.
- **A. Tempia Calvino**, "The EPFL Logic Synthesis Libraries: open-source tools for classical and emerging technologies", in Free Silicon Conference (FSiC), *scheduled*, 2024.
- **A. Tempia Calvino**, "Improving Technology Mapping for Standard Cells", at IBM Thomas J. Watson Research Center, 2024.
- **A. Tempia Calvino**, "Improving Delay-driven LUT Mapping with Boolean Decomposition", at Efinix Inc., 2024.
- **A. Tempia Calvino**, "Improving Delay-driven LUT Mapping with Boolean Decomposition", at AMD Inc. (Vivado team), 2023.
- **A. Tempia Calvino**, "Technology Mapping Using Multi-output Library Cells", at Google X, 2023.
- **A. Tempia Calvino**, "Improving Standard-Cell Design Flow using Factored Form Optimization", at Cadence Design Systems Inc., 2023.
- **A. Tempia Calvino**, "EPFL Benchmark Results Update", in International Workshop on Logic & Synthesis (IWLS), 2023.
- **A. Tempia Calvino**, "EPFL Benchmark Results Update", in International Workshop on Logic & Synthesis (IWLS), 2022.
- **A. Tempia Calvino**, "EPFL Benchmark Results Update", in International Workshop on Logic & Synthesis (IWLS), 2021.

Conference Talks:

- **A. Tempia Calvino**, "Practical Boolean Decomposition for Delay-driven LUT Mapping", in International Workshop on Logic & Synthesis (IWLS), 2024.
- **A. Tempia Calvino**, "Area-Oriented Resubstitution For Networks of Look-Up Tables", in International Workshop on Logic & Synthesis (IWLS), 2024.
- **A. Tempia Calvino**, "Scalable Logic Rewriting Using Don't Cares", in Design Automation and Test in Europe Conference (DATE), 2024.
- **A. Tempia Calvino**, "Algebraic and Boolean Methods for SFQ Superconducting Circuits", in Asian and South Pacific Design Automation Conference (ASP-DAC), 2024.
- **A. Tempia Calvino**, "In Medio Stat Virtus: Combining Boolean and Pattern Matching", in Asian and South Pacific Design Automation Conference (ASP-DAC), 2024.
- **A. Tempia Calvino**, "Technology Mapping Using Multi-output Library Cells", in IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2023.
- **A. Tempia Calvino**, "Improving Standard-Cell Design Flow using Factored Form Optimization", in ACM/IEEE Design Automation Conference (DAC), 2023.
- **A. Tempia Calvino**, "Technology Mapping Using Multi-output Library Cells", in International Workshop on Logic & Synthesis (IWLS), 2023.
- **A. Tempia Calvino**, "Depth-Optimal Buffer and Splitter Insertion and Optimization in AQFP Circuits", in Asian and South Pacific Design Automation Conference (ASP-DAC), 2023.
- **A. Tempia Calvino**, "Depth-optimal Buffer and Splitter Insertion and Optimization in AQFP Circuits", in International Workshop on Logic & Synthesis (IWLS), 2023.
- **A. Tempia Calvino**, "A versatile mapping approach for technology mapping and graph optimization", in Asian and South Pacific Design Automation Conference (ASP-DAC), 2022.
- **A. Tempia Calvino**, "From Logic to Gates: A Versatile Mapping Approach to Restructure Logic", in

International Workshop on Logic & Synthesis (IWLS), 2021.

Honors and Awards

- Best paper award at 2023 IFIP/IEEE 31st International Conference on Very Large Scale Integration (VLSI-SoC) for the paper"Synthesis of SFQ Circuits with Compound Gates".
- First place in the International Workshop on Logic & Synthesis (IWLS) Contest 2022: "Synthesis of small circuits for completely-specified multi-output Boolean functions represented using truth table".
- Best Student Paper Candidate at International Workshop on Logic & Synthesis 2021 (IWLS) for the paper "From Logic to Gates: A Versatile Mapping Approach to Restructure Logic".
- Best Poster Award at International Conference on Model-Driven Engineering and Software Development (MODELSWARD) 2021 for the paper "Direct Model-checking of SysML Models".
- EDIC I&C Ph.D. Fellowship, EPFL, 2020.

Teaching Assistantships

- Design Technologies for Integrated Systems, M.Sc. course, Fall 2023, EPFL.
- Digital System Design, B.Sc. course, Spring 2023, EPFL.
- Design Technologies for Integrated Systems, M.Sc. course, Fall 2022, EPFL.
- Real time embedded systems, M.Sc. course, Spring 2022, EPFL.
- Design Technologies for Integrated Systems, M.Sc. course, Fall 2021, EPFL.
- Real time embedded systems, M.Sc. course, Spring 2021, EPFL.
- Object-Oriented Programming, B.Sc. course, Spring 2018, Politecnico di Torino.
- Algorithms and Programming in C, B.Sc. course, Fall 2017, Politecnico di Torino.

Service and Leadership

Reviewer I reviewed articles for several top-tier conferences and journals such as TCAD, ICCAD, DATE, DAC, IWLS, DDECS, ISVLSI.

Service Maintainer of the EPFL Combinational Benchmark Suite. New updates and best results are presented annually at the International Workshop on Logic & Synthesis (IWLS). *Available at*: https://github.com/lsils/benchmarks.

Service Contributing and maintaining open-source software. Maintaining the EPFL logic synthesis libraries, *available at*: https://github.com/lsils/lstools-showcase and contributing to the logic synthesis tool ABC, *available at*: https://github.com/berkeley-abc/abc.

Member Graduate student member of IEEE and IEEE Young Professionals

Technical and Personal Skills

Domains of expertise

Logic synthesis, electronic design automation, digital design, microelectronics, algorithms, data structures, computer architectures.

Programming Languages

C, C++, VHDL, Verilog, Java, Python, TCL, Bash, LaTeX, and more.

Languages

- English, Italian, French